2 T826/827 Circuit Operation

This section provides a basic description of the circuit operation of the T826 transmitter and T827 exciter.

Note: Unless otherwise specified, the term "PGM800Win" used in this and following sections refers to version 2.00 and later of the software.

Refer to Section 6 where the parts lists, grid reference index and diagrams will provide detailed information on identifying and locating components and test points on the main PCB. The parts list and diagrams for the VCO PCB are in Part E.

The following topics are covered in this section.

2.1 Introduction

The individual circuit blocks which make up the T826 and T827 are:

- synthesiser
- VCO
- audio processor
- drive amplifier
- power amplifier (T826 only)
- voltage regulators.

Each of these circuit blocks is set in its own shielded compartment, formed as an integral part of the main chassis.

The configuration of the circuit blocks may be seen on a functional level in Figure 2.1 and Figure 2.2. Refer to the circuit diagrams in Section 6.2 (T826) or 6.3 (T827) for more detail.

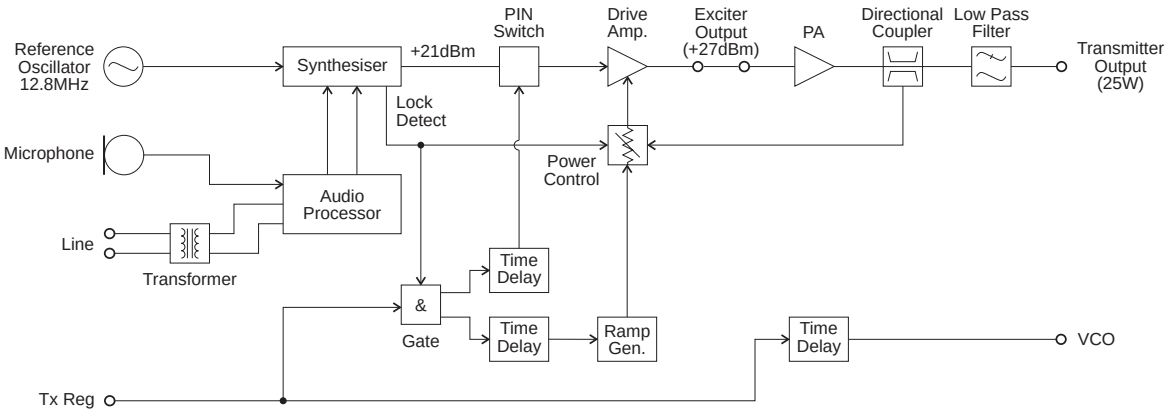

Figure 2.1 T826 High Level Block Diagram

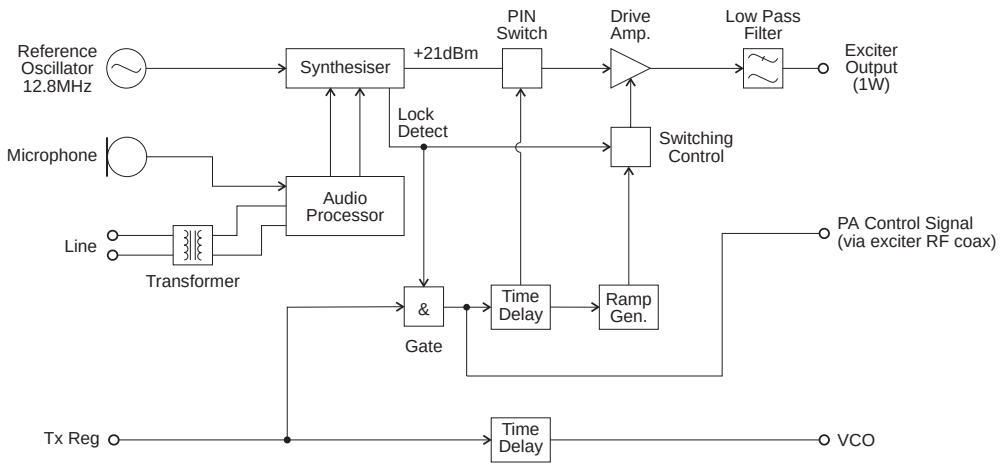

Figure 2.2 T827 High Level Block Diagram

2.2 Microcontroller

(Refer to the microcontroller circuit diagram (sheet 8) in Section 6.2 or 6.3.)

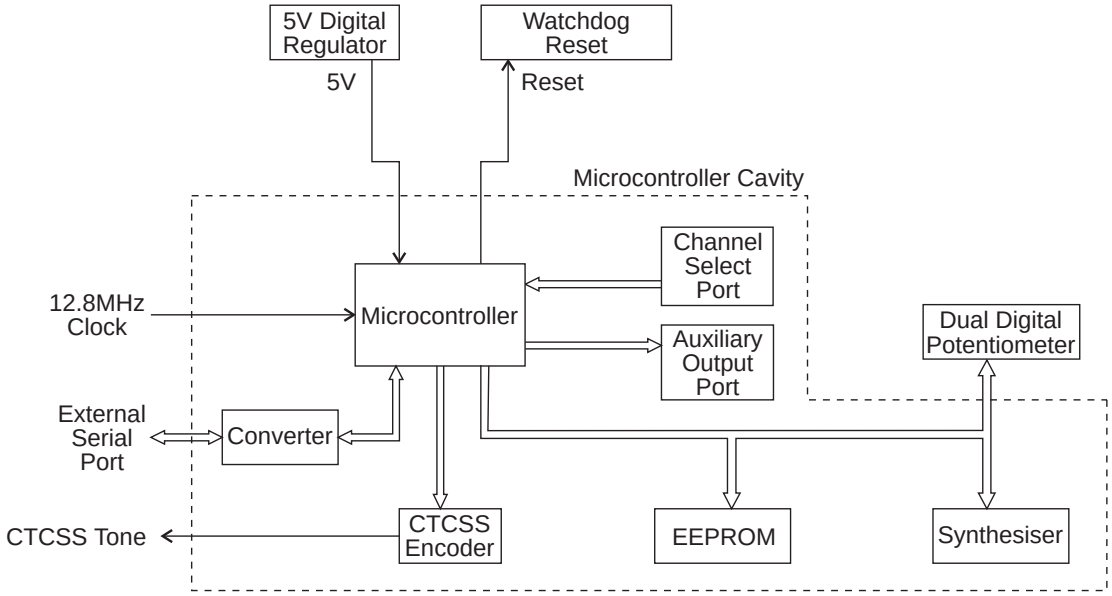

Figure 2.3 T826/827 Microcontroller Block Diagram

Overall system control of the T826/827 is accomplished by the use of a member of the 80C51 family of microcontrollers (IC810). It runs from internal ROM and RAM, thus leaving all four ports free for input/output functions.

Non-volatile data storage is achieved by serial communication with a 16kBit EEPROM (IC820). This serial bus is also used by the microcontroller to program the synthesiser (IC740) and deviation control EPOTS (IC220).

The main tasks of the microcontroller are as follows:

- program the synthesiser and EPOT;
- interface with the PGM800Win programming software at 9600 baud via the serial communication lines on D-range 1 (PL100) & D-range 2;
- monitor channel change inputs from D-range 2;
- generate timing waveforms for CTCSS encoding;
- coordinate and implement timing control of the exciter/transmitter;
- control the front panel "Supply" LED.

2.3 Synthesised Local Oscillator

(Refer to the synthesiser circuit diagram (sheet 7) in Section 6.2 or 6.3 and the VCO circuit diagram in Part E.)

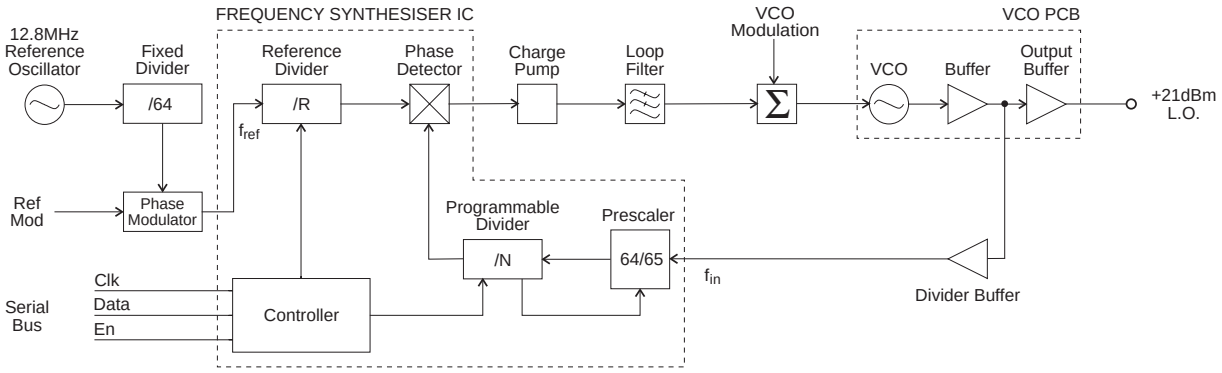

Figure 2.4 T826/827 Synthesiser Block Diagram

The synthesiser (IC740) employs a phase-locked loop (PLL) to lock a voltage controlled oscillator (VCO) to a given reference frequency. The synthesiser receives the divider information from the control microprocessor via a 3 wire serial bus (clock, data, enable). When the data has been latched in, the synthesiser processes the incoming signals from the VCO buffer (f_{in}) and the phase modulator (f_{ref}).

A reference oscillator at 12.8MHz (=IC700) is buffered (IC710 pins 5 & 6) and divided down to 200kHz (IC730). This 200kHz square wave is then summed with the modulating audio and passed to an integrator (IC720 pins 9 & 8, Q710, Q720). This produces a ramping waveform which is centred around a DC level determined by the incoming audio. IC720 pins 5 & 6 perform as a comparator, ultimately producing a phase-modulated 200kHz square wave. This is followed by another phase shifting stage (IC720 pins 3 & 4, Q730, Q740), before being divided down to 6.25kHz or 5kHz within the synthesiser IC (IC740).

A buffered output of the VCO (Q795) is divided with a prescaler and programmable divider which is incorporated into the synthesiser chip (IC740). This signal is compared with the phase modulated reference signal at the phase detector (also part of the synthesiser chip). The phase detector outputs drive a balanced charge pump circuit (Q760, Q770, Q775, Q780, Q785) and active loop filter (IC750 pins 5, 6 & 7) which produces a DC voltage between 0V and 20V to tune the VCO. This VCO control line is further filtered to attenuate noise and other spurious signals. Note that the VCO frequency increases with increasing control voltage.

If the synthesiser loop loses lock, a pulsed signal appears at LD (pin 2) of IC740. This signal is filtered and buffered by IC750 pins 1, 2 & 3, producing the Lock-Detect signal used to shut off the power supply to the drive amplifier. IC750 pin 1 is at 20V when the synthesiser is out of lock.

2.3.1 Two Point Modulation

Frequency modulation occurs by modulating both the VCO input and the synthesiser reference input. This process is called two point modulation and ensures a flat modulation response from 67Hz to 3kHz (2.55kHz for narrow bandwidth).

The PLL has a fast response time, allowing a Tx key-up time of <30ms. Because of this fast response time the PLL sees lower modulation frequencies superimposed on the VCO as an error and corrects for it, resulting in no modulation on the carrier. At modulation frequencies greater than 300Hz the loop cannot correct fast enough and modulation is seen on the carrier. The response of the loop to VCO modulation is shown by f_2 in Figure 2.5 below.

To achieve low frequency modulation, the reference oscillator is also modulated so that the phase detector of IC740 detects no frequency error under modulation. Thus, the synthesiser loop will not attempt to correct for modulation and the audio frequency response of the transmitter remains unaffected. The response of the loop to reference frequency modulation is shown by f_1 in Figure 2.5.

The reference modulation is controlled by a 256-step 10k electronic potentiometer (EPOT) which is adjustable via PGM800Win. The EPOT is made up of 256 resistive sections (representing approximately 39Ω each) which can be individually addressed by the microcontroller. Each section can be switched in or out of circuit to achieve the required total resistance, thus giving control of the reference modulation.

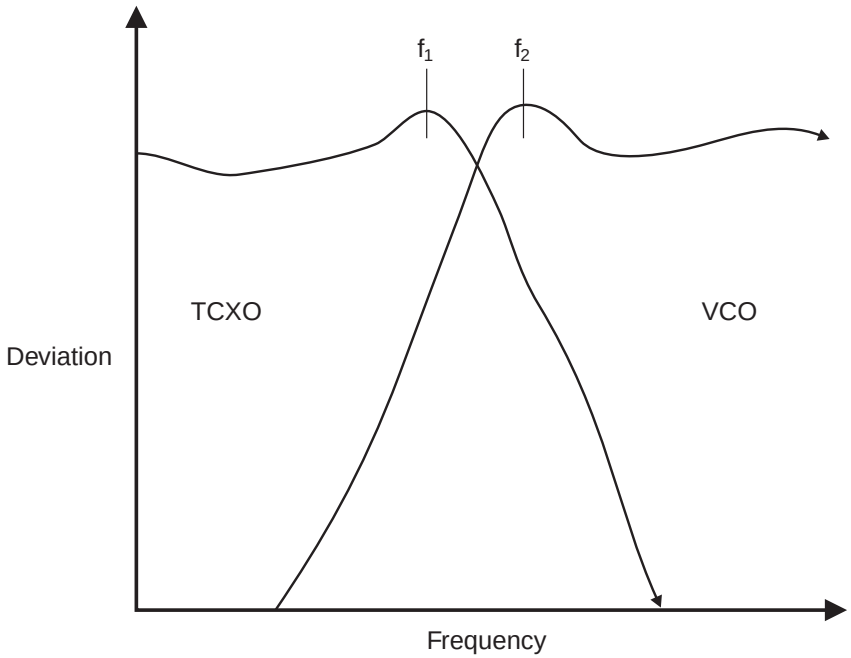

Figure 2.5 T826/827 Two Point Modulation

2.4 VCO

(Refer to the VCO circuit diagram in Part E.)

The VCO transistor (Q1) operates in a common source configuration, with an LC tank circuit coupled between its gate and drain to provide the feedback necessary for oscillation. The VCO control voltage from the loop filter (IC750 pin 7) is applied to the varicaps (D1-D6) to facilitate tuning within an 8MHz band of frequencies. A trimcap (&VC1-TX) is used for coarse tuning of the VCO. The output from the oscillator circuit drives a cascode amplifier stage (Q2, Q3) which supplies +10dBm (typically) to a further stage of amplification, Q5. This is the final amplifier on the VCO PCB, and delivers +21dBm (typically) to the exciter drive amplifier.

A low level "sniff" is taken from the output of Q3 and used to drive the divider buffer (Q795) for the synthesiser (IC740).

The VCO operates at the actual output frequency of the exciter, i.e. there are no multiplier stages. The VCO is modulated by superimposing the audio signal onto the control voltage and by phase modulating the reference signal.

2.4.1 VCO Supply

The VCO is supplied from two switched +9V supplies under the control of the Tx-Reg. supply.

The VCO (Q1) and buffer amplifier (Q2 & Q3) are supplied from one +9V switched supply by Q540 via the capacitor multiplier (Q550, C550).

The output amplifier is supplied from the other +9V supply by Q520, Q530, and Q510.

A delay circuit holds the VCO on for a short time after the Tx-Reg. supply has been switched off. This is to allow the RF power circuits (both exciter and PA) to ramp down in the correct manner before the VCO is switched off.

2.5 Audio Processor

(Refer to the audio processor circuit diagram (sheet 2) in Section 6.2 or 6.3.)

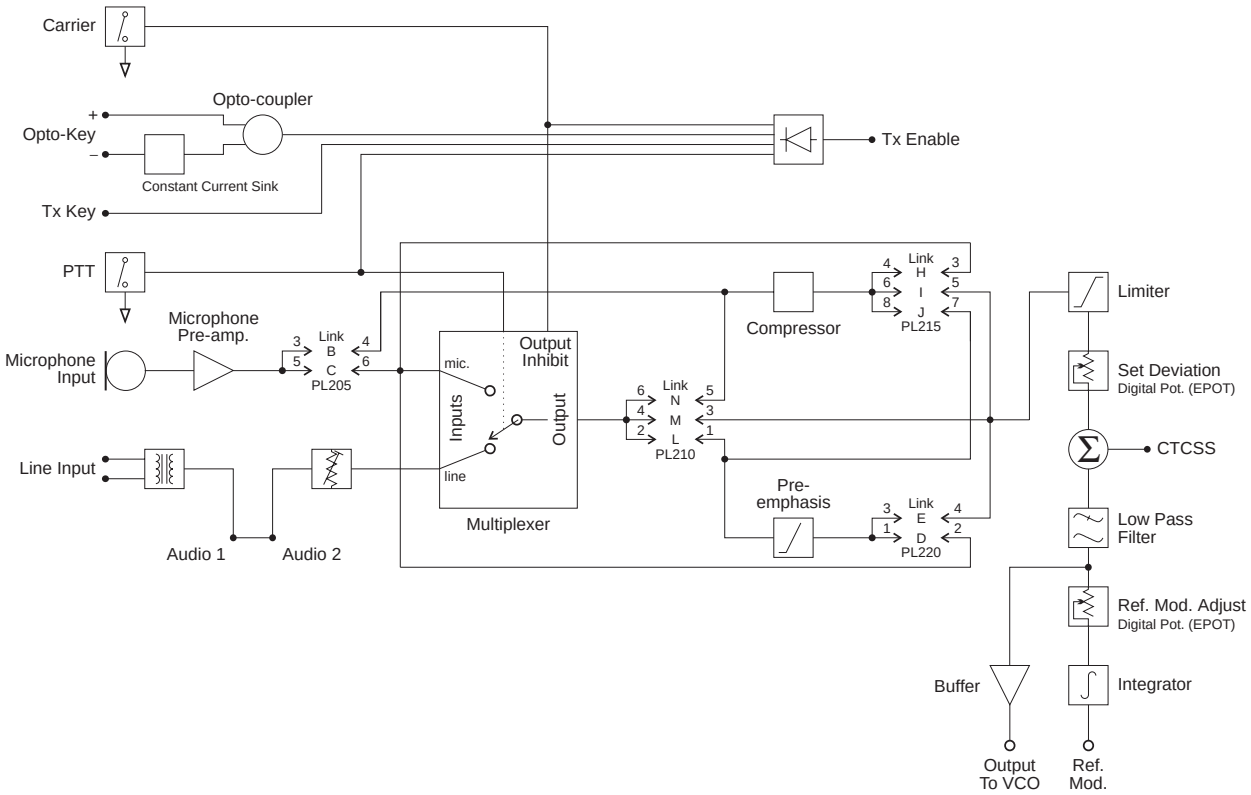

Figure 2.6 T826/827 Audio Processor Block Diagram

2.5.1 General

The audio processor comprises several link selectable circuit blocks which may be configured in a variety of combinations to suit individual requirements. The pre-emphasis network and compressor may be linked individually or cascaded between either or both audio inputs and the limiter.

Refer to Section 3.5.1 for linking details.

2.5.2 Audio Inputs

Two audio inputs are available: one from a 600 ohm balanced (or unbalanced) line, and the other from a local microphone. The microphone signal is passed first to a pre-amplifier (Q210) and ultimately to a multiplexer (IC240), but in between may pass through the compressor (depending on the linking details). The line transformer is also connected to the multiplexer and is disabled by the microphone PTT switch.

A third input for external CTCSS tones is also provided.

2.5.3 Keying Inputs

There are four ways to key the exciter:

- pulling the Tx-Key line low (pin 13 on D-range 1 [PL100]) at the rear of the set);
- pushing the "Carrier" button on the front panel - this will inhibit all audio;
- using the PTT button on the local microphone, disabling audio from the line;
- via the opto-key inputs (pins 11 and 12 on D-range 1 [PL100]) when electrical isolation is required. This features a constant current sink (Q270) to ensure reliable activation of the opto-coupler (IC250) at low keying voltages.

2.5.4 Compressor (Automatic Level Control (ALC))

The input signal is fed via a current controlled attenuator (Q230, Q220) to a high gain stage (IC230) from which the output signal is taken. This signal is passed to a comparator (IC230) which toggles whenever the audio signal exceeds a DC threshold determined by RV220. Thus, the comparator produces a square wave whose mark-space ratio is determined by the amplitude of the audio signal. This square wave pumps up the reservoir capacitor (C233) which controls the attenuator (Q230, Q220), thus completing the feedback loop.

The compression level is set by adjustment of the comparator threshold (RV220).

Note: Although the high dynamic range of the compressor allows the use of very low audio signal levels, such conditions will be accompanied by a degradation of the signal-to-noise ratio. Very low audio input levels should therefore be avoided where possible.

2.5.5 Outputs To Modulators

The output signal from the limiter (IC210, IC230) is added with a CTCSS tone at a summing amplifier (IC260). The signal is then low pass filtered (IC260) and split to supply the two modulators.

Since the VCO modulator is a true frequency modulator, its audio is simply buffered (IC260). The reference modulator, however, is a phase modulator and its audio must first be integrated (IC210).

It is vital that the audio levels to the modulators are accurately set, ***relative to each other***. Hence the inclusion of level adjustment in the reference modulator path. Once set, adjustments to absolute deviation may be made only by IC220, a 256-step 10k electronic potentiometer (EPOT), which is controlled via PGM800Win. The EPOT is made up of 256 resistive sections (representing approximately 39Ω each) which can be individually addressed by the microcontroller. Each section can be switched in or out of circuit to achieve the required total resistance, thus adjusting the absolute deviation level.

2.6 Power Supply & Regulator Circuits

(Refer to the regulators circuit diagram (sheet 6) in Section 6.2 or 6.3.)

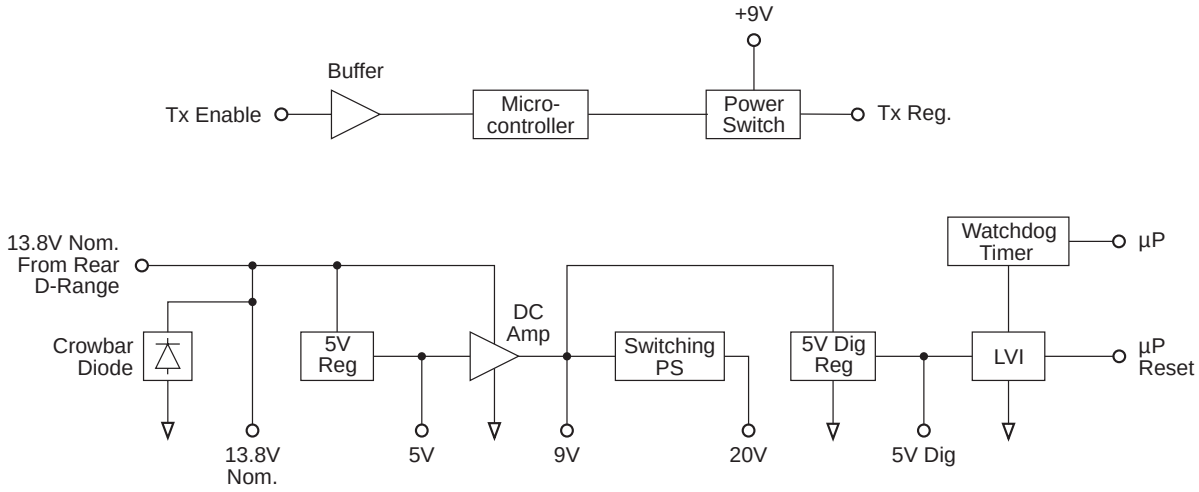

Figure 2.7 T826/827 Power Supply & Regulators Block Diagram

The T826 and T827 are designed to operate from a 10.8-16V DC supply (13.8V nominal). A 5.3V regulator (IC630) runs directly from the 13.8V rail, driving much of the synthesiser circuitry. It is also used as the reference for a DC amplifier (IC640, Q630, Q620) which provides a medium current capability 9V supply.

A switching power supply (Q660, Q670) runs from the 9V supply and provides a low current capability +20V supply. This is used to drive the synthesiser loop filter (IC750), giving a VCO control voltage range of up to 20V, and the Lock-Detect amplifiers.

Ultimate control of the transmitter is via the Tx-Reg. supply, switched from 9V by Q610. This is enabled via the Tx-Enable signal from the audio processor, and microprocessor.

A crowbar diode is fitted for protection against connection to a power supply of incorrect polarity. It also provides transient overvoltage protection.

Note: A fuse must be fitted in the power supply line for the diode to provide effective protection.

2.7 Transmit Timers

The transmit tail timer, transmit timeout timer and transmit lockout timer can all be set from PGM800Win. The fields for setting these are found on the system information page. These three timers operate as follows (refer also to Figure 2.8):

Timer	Function	Adjustment
Transmit Tail	Sets the tail time during which the transmitter stays keyed after the external key source has been removed.	0-5 seconds in 100ms steps[a]
Transmit Timeout	Sets the maximum continuous transmission time. Once the timer has timed out, the transmitter must be keyed again, unless prevented by the transmit lockout timer.	0-300 seconds[b] in 10 second steps
Transmit Lockout	Sets the period of time that must elapse after a timeout before the transmitter can re-transmit. Once the timer has timed out, the transmitter can be keyed again.	0-60 seconds in 10 second steps

a. Adjustable in 20ms steps in PGM800Win version 2.12 and later.
b. Adjustable from 0 to 600 seconds in PGM800Win version 2.12 and later.

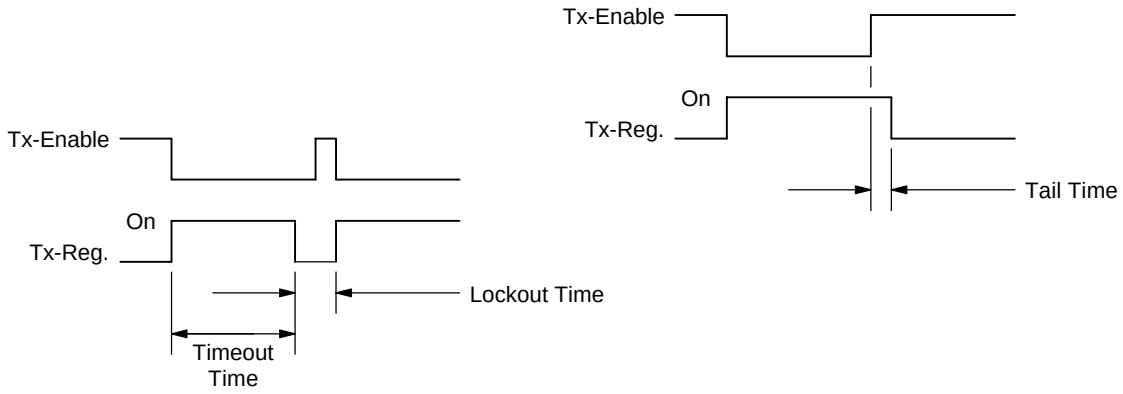

Figure 2.8 T826/827 Transmit Timers

2.8 T826 Drive Amplifier & PA

(Refer to Figure 2.1 and the exciter and PA circuit diagrams (sheets 3 & 4) in Section 6.2.)

The output power of the PA is maintained at a constant level via a power control loop applied to the two-stage, wide band exciter amplifier (Q307, Q312). The forward and reverse RF power levels are sensed via a dual directional coupler and detector diodes (D440, D441 in the PA cavity). The detected DC signals are summed with the "power set" level and fed to the control integrator (IC310 pins 1, 2 & 3). The output control voltage is buffered by Q309 and Q315, and applied to the collectors of the wide band exciter amplifiers.

Note: Forward and reflected power signals are summed so that, under high VSWR, the power control will turn the output RF level down.

The maximum output power of the transmitter is limited by a voltage clamp circuit (consisting of a potential divider formed by R369//R374 and R375//R359//R360) which turns on Q308, clamping the control voltage to approximately 7.8V. When the maximum operating temperature is exceeded, the clamp voltage is reduced to approximately 5.7V by removing R359//R360 from the circuit (see below).

To reduce the spurious output level when the synthesiser is out-of-lock, the Tx-Reg. and Lock-Detect signals are gated to inhibit the PA control circuit and to switch off the RF signal at the input to the drive amplifier. The RF input signal is switched by a PIN switch attenuator (D300, D301, D302).

Cyclic keying control is provided by additional circuitry consisting of several time delay, ramp and gate stages:

- Q305, IC310 power ramping
- Q304, Q305 Tx-Reg. and $\overline{\text{Lock-Detect}}$ gate
- Q300, Q301, Q302 delay and PIN switch drive.

This is to allow the RF power circuits (both exciter and PA) to ramp up and down in a controlled manner so that minimal adjacent channel interference is generated during the transition.

The output of the wide band amplifier is approximately 550mW (+27.5dBm) for an input of 65mW (+18dBm) when the power control is set to maximum.

Note: The VCO output level of 125mW (+21dBm) is attenuated by a 3dB attenuator (R517, R518 & R519) in the VCO cavity. This provides good VCO/exciter isolation as well as the correct exciter drive level.

A temperature sensor (R480) is provided so that the RF output power can be reduced to a preset level when a set temperature is exceeded. This is a protection circuit (IC310 pins 5, 6 & 7, Q311) to prevent overheating, as the unit is ***not*** rated for continuous operation at high temperatures (refer to Section 1.2.3 for duty cycle specifications). RV302 sets the PA output power while under high temperature fold-back conditions.

The output of the temperature-sense comparator (IC310 pin 7) also feeds to a secondary shutdown clamp circuit (Q303, Q360, Q308). The clamp voltage is set to approximately

5.7V by the potential divider R369//R374 and R375 when the maximum operating temperature is exceeded. This ensures that the temperature shutdown will reduce the output power even if the power control circuit is in an open loop condition.

The attenuator (R410, R411 & R412) aids in reducing exciter/PA interaction while also ensuring a reasonable match for Q312.

The RF output from the exciter is fed to the driver stage (Q415) and then to the final (Q425). The DC supply is fed to the final via a low pass filter with special low frequency decoupling.

The directional coupler provides the required feedback for the power control loop while the harmonics are attenuated by the low pass filter.

2.9 T827 Exciter Drive Amplifier

(Refer to Figure 2.2 and the exciter circuit diagram (sheet 3) in Section 6.3.)

A two-stage, wide band amplifier (Q320, Q321) provides an output level of approximately 1W (+30dBm) for an input of 125mW (+21dBm) from the VCO. IC300 pins 5, 6 & 7, Q301 and Q302 provide a 10.5V regulated supply for the exciter.

To reduce the spurious output level when the synthesiser is out-of-lock, the Tx-Reg. and Lock-Detect signals are gated to inhibit the exciter control circuit and to switch off the RF signal at the input to the drive amplifier. This is achieved by a PIN switch attenuator (D320, D321, D322).

Cyclic keying control is provided by additional circuitry consisting of several time delay, ramp and gate stages:

- Q300, IC300 pins 5, 6 & 7 — power ramping
- Q380, Q381 — Tx-Reg. and $\overline{\text{Lock-Detect}}$ gate
- Q365, Q366, Q367, Q368 — delay and PIN switch drive.

This is to allow the RF power circuits (both exciter and PA) to ramp up and down in a controlled manner so that minimal adjacent channel interference is generated during the transition.

R517, R518 and R519 form a 3dB attenuator to provide good VCO/drive amplifier isolation.

The output attenuator (R337, R338, R339) assists in reducing exciter/PA interaction while also ensuring a good match for Q321.

Note: The exciter provides a DC control signal to the PA via the RF coax. This is injected via %L382.